# Modeling of Current Lag in GaAs IC's

**W. R. Curtice*, J. H. Bennett**, D. Suda** and B. A. Syrett*****

***W. R. Curtice Consulting, 5 Berkshire Drive, Princeton Junction, NJ, 08550 USA**
****Nortel Technology, Northern Telecom, POB 3511 Station C,Ottawa, ON K1Y 4H7, Canada**
***** Carleton University, Ottawa, ON, Canada K1S 5B6**

ABSTRACT

Leakage currents, thermal effects and deep-level traps cause significant current lag effects in GaAs MESFETs. A conventional, MESFET large-signal, equivalent-circuit model has been modified to simulate these effects and used to improve the design of GaAs digital control and rf switching circuits. Both gate lag and drain lag are simulated as well as over-shoot or under-shoot behavior.

## I. Introduction

The purpose of this work is to extend the large-signal FET model capability to include simulating the gate and drain lag phenomena and self-heating effects for the GaAs MESFETs. The modeling of self-heating is well understood. Drain-lag behavior and circuit models have been demonstrated by Lee and Forbes[1] and by Kunihiro and Ohno[2]. But, neither of these circuits will accommodate the gate-lag behavior observed in the Nortel FETs.

The lag behavior, the modified GaAs MESFET model and simulations using this model will be described. The model has been installed in HP-EEsof Series IV and operates in both the frequency domain (for harmonic balance operation) and the time domains (for transient simulation). This paper is concerned primarily with gate lag effects, since drain lag and its simulation have been previously studied.

## II. The Evaluation of Current Lag Parameters

We classify the gate lag tests as Type I **,** where Voff, the value of Vgs below pinch-off is varied , and Type II, where Von, the value of Vgs in the on state is varied , or,

| Test Type | Von | Voff |
|---|---|---|
| **I** | **0.1 V** | **-2,-3 & -5 V** |
| **II** | **0.1, 0.4 & 0.5 V** | **-3 V** |

Type I tests produce current lag with a long time constant, which is probably associated with gate leakage current and a DLT, or deep-level trap[3]. Type I lag is illustrated in Figure 1 where a time constant of about 20 ms is seen for Voff= -5 V.

Type II tests produces lag with shorter time constants (10 to 100 us) and this is probably associated with gate forward conduction in conjunction with several shallower DLTs.

Because several time constants are present, evaluation of a particular circuit's tolerance to lag usually requires successive simulations each using one time-constant lag effect. Usually, one time constant has the largest effect upon the circuit's operation. However, the lag circuit could be duplicated for simultaneous operation with two different time constants. This has not been necessary.

The lag coefficient is evaluated for each individual time constant. This is accomplished by evaluating the lag coefficient that reproduces the lag current changes using the model to be described next.

## III. The Large-Signal Model Modified to Include Current Lag

The topology of the N_FET shown in Figure 2 is similar to most conventional large-signal FET models but some additional circuits have been added to accommodate self-heating effects, drain lag and gate lag. The current control characteristic is due to Curtice and Ettenberg [4] and improved capacitance functions are used.

Two lag circuits have been added. The first is a drain lag circuit. Its function is to sample the output voltage and feed back to the gate a fraction of that voltage. The second lag circuit is added to the gate and performs the same function. Each circuit is an RC circuit and has a characteristic time constant and feed-back factor which are the lag parameters. The circuits model over-shoot behavior as well as under-shoot behavior . These circuits have been

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

added in such a manner as not to disturb the transistor's dc control characteristics.

## IV. Current Lag Simulations

The network for the 6x50 FET and the test bench for simulation of gate lag effects are shown in Figures 3 and 4, respectively. Using the gate-lag time constant, T_GL, of value 1 ms , Figure 5 shows current simulations for values of gate-lag coefficient of GL_C = -0.1, 0. and + 0.1 . Vds has been taken low, to eliminate thermal lag effects.

Drain lag effects are simulated in a similar manner but by pulsing the drain voltage rather than the gate voltage and setting the drain lag parameters, DL_C and T_DL. Drain lag data often contains significant contribution due to transient thermal behavior and this must be separately evaluated. Several time constant are often involved for each lag effect.

## V. Lag in FET Switches for RF

It was found possible to simulate the same behavior of a GaAs MESFET used as a switch for 10 GHz rf signals. Figure 6 shows a case with GL_C = .1 and T_GL= 1us. Gate lag reduces the transmitted signal level significantly.

## VI. Lag in Digital Circuits

The control circuit for the rf switch consists of 15 transistors of various sizes whose purpose is to provide the logic control of FETs which determine rf signal routing. Figure 7 shows the simulated OUT and OUTNOT waveforms for transistors with no lag effects. Figure 8 shows a simulated case of poor switching waveforms due to lag. Similar waveforms were measured.

## References


[1]. Lee and Forbes, "A Self-Backgating GaAs MESFET Model for Low-Frequency Anomalies," IEEE Transactions on Electron Devices, Vol. 37, No. 10, pp. 2148-2157, October 1990.

[2] Kunihiro and Ohno, "A Large-Signal Equivalent Circuit Model for Substrate-Induced Drain-Lag Phenomena in HJFETs," IEEE Transactions onElectron Devices, Vol. 43, No. 9, pp. 1334-1342, September 1996.

[3] Li and Dutton, "Numerical Small-Signal AC Modeling of Deep-Level-Trap Related Frequency-Dependent Output Conductance and Capacitance for GaAs MESFETs on Semi-insulating Substrates," IEEE Transactions on Electron Devices, Vol. 38, No. 6, p. 1285, June 1991.

[4] Curtice and Ettenberg, "A Nonlinear GaAs FET Model for Use in the Design of Output Circuits for Power Amplifiers," IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-33, pp. 1383-1394, December 1985.


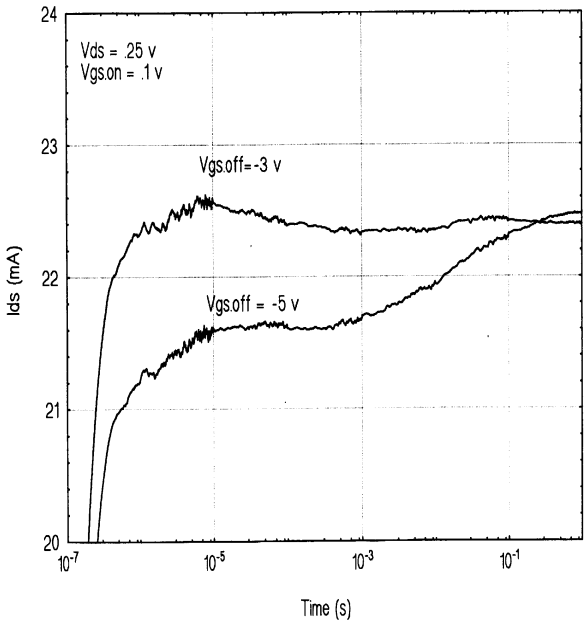


Figure 1. Lag Data for 6x50 FET

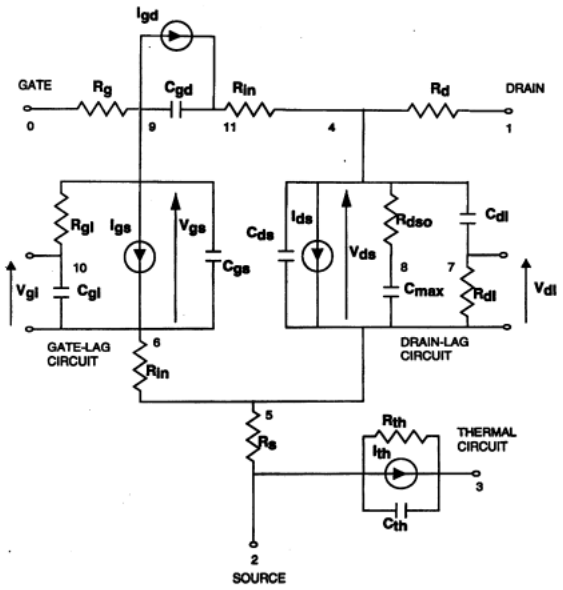


Figure 2. FET Model

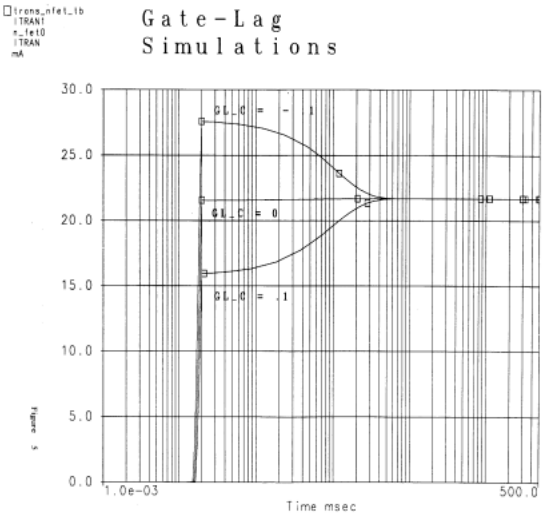


Figure 5. Gate-Lag Simulations

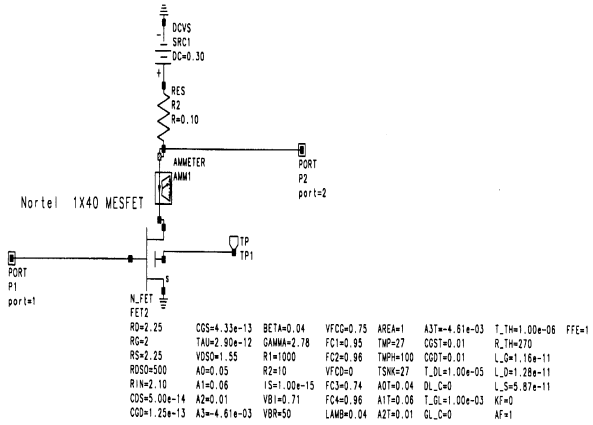


Figure 3. Schematic Layout

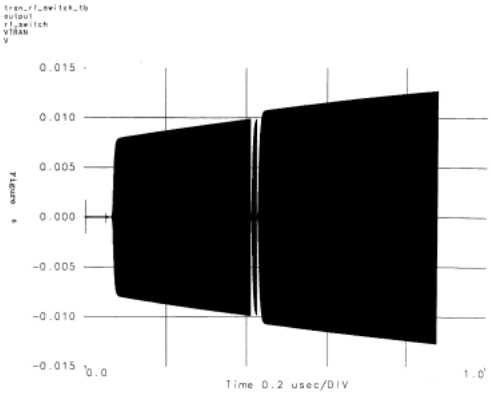


Figure 6. Rf Switch Output Simulation

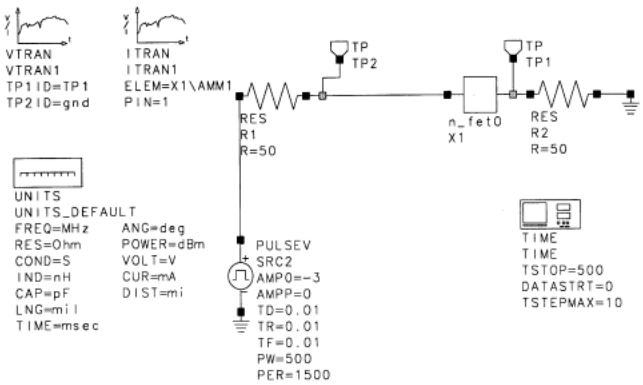


Figure 4. Test Bench

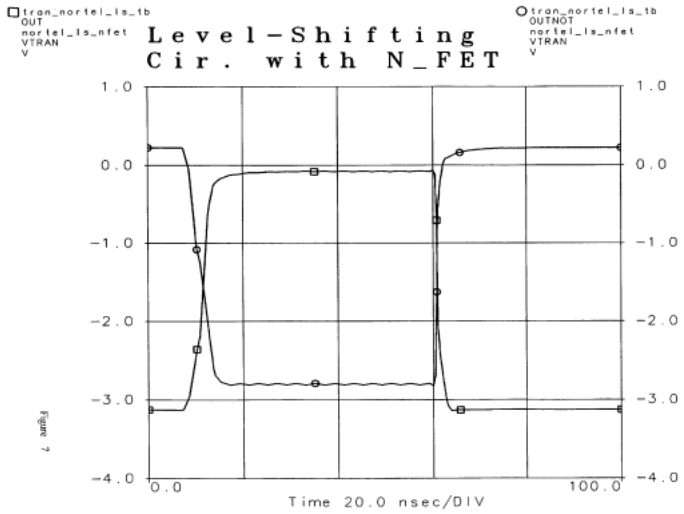


Figure 7. OUT and OUTNOT with zero lag coefficients

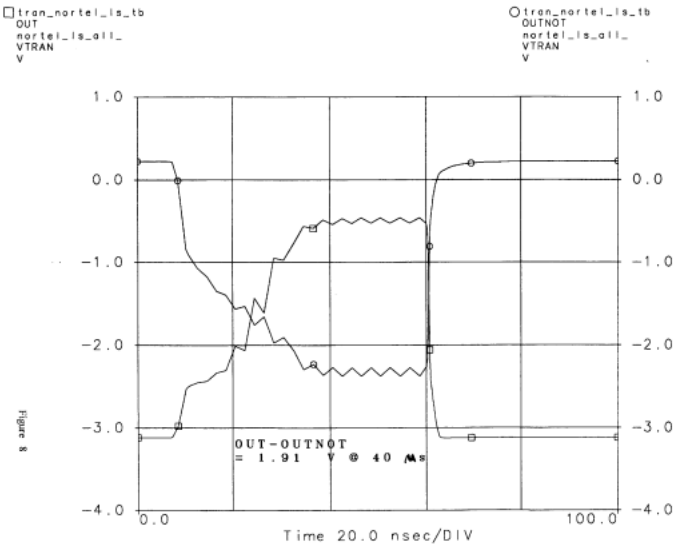


Figure 8. OUT and OUTNOT with gate lag coefficient of 0.15 .Time constant is 1 ms.